IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Arthur R. Alexander, et al.	§	Group Art Unit:	2841
		§		
Serial No.:	10/630,886	§		
		§	Examiner:	Tuan T. Dinh
Filed:	July 30, 2003	§		
		§		
For:	PROVIDING A RESISTIVE ELEMENT BETWEEN REFERENCE PLANE LAYERS IN A CIRCUIT BOARD	§	Atty. Dkt. No.:	11279 (NCR)
		§		
		§		
		§		

Mail Stop: Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF IN SUPPORT OF APPEAL

Dear Sir:

This is a brief in support of Applicant's Notice of Appeal filed on October 19, 2006, in response to the final rejection dated May 19, 2006, in this matter. In addition, Applicant filed a pre-appeal brief with the notice of appeal. On December 4, 2006, a Notice of Panel Decision was issued stating the case should proceed to the Board of Patent Appeals and Interferences. Therefore, Applicant is filing this brief along with any required fee(s).

(1) REAL PARTY IN INTEREST

The real party in interest in this matter is NCR Corporation, Dayton, Ohio, by virtue of an assignment recorded at reel 014366, frame 012-014, on July 30, 2003.

(2) RELATED APPEALS AND INTERFERENCES

Applicant is aware of no other active appeals or interferences related to this application.

(3) STATUS OF CLAIMS

Claims 15 and 25 are currently pending in this application. Claims 15 and 25, having been rejected two or more times, are under appeal. The text of the claims, as currently pending, is attached as an appendix to this brief.

(4) STATUS OF AMENDMENTS

On October 19, 2006, Applicant filed a notice of appeal with a pre-appeal brief in response to the final rejection dated May 19, 2006. In a Notice of Panel Decision from Pre-Appeal Brief Review mailed on December 4, 2006, the Panel rejected Applicant's arguments and stated the case should proceed to the Board of Patent Appeals and Interferences.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 15 recites a circuit board comprising (e.g., page 4, paragraph 20; Fig. 1, element 100), a first reference plane layer (e.g., page 5, paragraph 20, page 11, paragraph 45; Fig. 7, elements 108), a second reference plane layer (e.g., page 5, paragraph 20, page 11, paragraph 45; Fig. 7, elements 112), a dielectric layer between the first and second reference plane layers (e.g., page 5, paragraph 21; Fig. 7, element 110), a decoupling capacitor having first and second electrodes (e.g., page 11, paragraph 45; Fig. 7, elements 300, 302, and 304) and a discrete resistor having first and second electrodes (e.g., page 11, paragraph 45; Fig. 7, element 400), the resistor's first electrode electrically connected to the

first reference plane layer, the resistor's second electrode electrically connected to the decoupling capacitor's first electrodes, and the decoupling capacitor's second electrode electrically connected to the second reference plane layers (e.g., page 11, paragraph 45; Fig. 7, elements 108, 400, 302, 304, and 112).

Independent claim 25 recites a system comprising an integrated circuit device (e.g., page 5, paragraph 20; Fig. 1, elements 130) and a circuit board on which the integrated circuit device is mounted (e.g., page 4, paragraph 20; Fig. 1, element 100), the circuit board comprising a first reference plane layer (e.g., page 5, paragraph 20, page 11, paragraph 45; Fig. 7, elements 108), a second reference plane layer (e.g., page 5, paragraph 20, page 11, paragraph 45; Fig. 7, elements 112), a dielectric layer between the first and second reference plane layers (e.g., page 5, paragraph 21; Fig. 7, element 110), a decoupling capacitor having first and second electrodes (e.g., page 11, paragraph 45; Fig. 7, elements 300, 302, and 304) and a discrete resistor having first and second electrodes (e.g., page 11, paragraph 45; Fig. 7, element 400), the discrete resistor's first electrode electrically connected to the first reference layer, the discrete resistor's second electrode electrically connected to the decoupling capacitor's first electrode, and the decoupling capacitor's second electrode electrically connected to the second reference layer (e.g., page 11, paragraph 45; Fig. 7, elements 108, 400, 302, 304, and 112).

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Independent claim 15 is rejected under 35 USC § 102(b) as being anticipated by Sunahara (U.S. Patent No. 6,153,290).

B. Independent claim 25 is rejected under 35 USC § 103(a) as being unpatentable over Sunahara in view of Chakravorty (U.S. Patent No. 6,611,419).

(7) ARGUMENT

Both rejected claims should be allowed over the cited reference for the reasons set forth below.

A 35 USC § 102(b) Rejection of Claim 15 by Sunahara

Sunahara does not show or suggest "a first reference plane layer," or "a second reference plane layer," or "a dielectric layer between the first and second reference plane layers," or "the resistor's first electrode electrically connected to the first reference plane layer," or "the decoupling capacitor's second electrode electrically connected to the second reference plane layers," as required by Applicant. The Office asserts that Sunahara teaches reference plane layers in column 5, line 31 and Fig. 1, elements 17 and 14. (See Office Action mailed May 19, 2006, page 2, paragraph 2.) Applicant disagrees. Sunahara identifies these structures as "wiring conductors" and states that "laminate 9 is provided with wiring conductors 13, 14, 15, 16, 17, and 18 for completing wiring among the capacitor 10, the inductor 11 and the resistor 12, and outer terminal conductors 19a and 19b ...." (Col. 5, lines 34-37.) Sunahara's wiring conductors (14, 17) are clearly not equivalent to Applicant's requirement for "reference plane layers." Applicant teaches "a circuit board ... has multiple layers of signal wires or conductors and power or ground reference planes." (Application, page 5, paragraph 20.) Applicant teaches the presence of two distinct types of structures, one being signal wires or conductors and the other being power or ground reference planes. Not only do they have different functions but they also have different physical attributes. Signal wires or conductors transmit signals over a wire or conductors. The reference planes are more substantial than a wire or conductor and provide sources for power or ground. Sunahara's wiring conductors are clearly signal wires or conductors. They are not planes as required by Applicant. In Fig. 1, Sunahara depicts two individual wiring conductors (16 and 17) on the same layer. The Office selected conductor 17 and asserted that it is equivalent to Applicant's reference plane layer. However, Sunahara never uses the terms "ground" or "power" and there is no teaching regarding reference planes. Sunahara shows conductor 17 as an individual wiring conductor that simply runs between a resistor and a via structure. Applicant

expressly distinguishes between signal wires or conductors and reference planes and requires a reference plane layer. A person of ordinary skill in the art would conclude that Sunahara's wiring conductor is indeed a signal wire and not a reference plane as required by Applicant. Therefore, all of the elements of Applicant's claim that require a reference plane layer are missing from Sunahara. Anticipation under 35 U.S.C. §102 is established only when a single prior art reference discloses each and every element of the claimed invention. RCA Corp. v. Applied Digital Data Systems, Inc., 221 USPQ 385 (Fed Cir. 1984). The rejection of Applicant's claim as being anticipated by Sunahara is thus improper and Applicant asks the Board to reverse this rejection.

B 35 USC § 103(a) Rejection of Claim 25 over Sunahara and Chakravorty

Neither Sunahara nor Chakravorty show or suggest "a discrete resistor having first and second electrodes, the discrete resistor's first electrode electrically connected to the first reference layer," as required by Applicant. The Office relies on Sunahara to teach this element but Applicant has shown above that Sunahara fails to teach the use or presence of a reference layer. Therefore, Sunahara can not teach a discrete resistor's first electrode electrically connected to a first reference layer, as required by Applicant. Chakravorty does not use the term "resistor" or teach the presence of a resistor. Chakravorty also fails to teach the required element.

To establish a *prima facie* case of obviousness, among other requirements, the combined references must teach or suggest all elements of the claimed subject matter. As shown above, the combined references fail to teach or suggest all the elements of Applicant's claim, therefore the Office has failed to establish a *prima facie* case of obviousness. The rejection is thus improper and Applicant asks the Board to reverse the rejection.

B. Conclusion

Neither Sunahara nor Chakravorty, together or separately, show or suggest all of the elements of Applicant's claimed invention. Therefore, these rejections are improper. Applicant asks the Board to reverse the rejections and to allow the claims.

Please apply any charges or credits that might be due, except the issue fee, to the NCR Corporation deposit account number 14-0225.

Respectfully submitted,

Date February 27, 2007

(Electronically Filed)

/Harden E. Stevens, III/

Harden E. Stevens, III
Agent for Applicant
Reg. No. 55,649

NCR Corporation
Law Department
1700 South Patterson Blvd.
Dayton, Ohio 45479

Tel. No. (803) 939-6505
Fax No. (803) 939-5099
Email: ss133111@ncr.com

(8) APPENDIX - Listing of Current Claims

1. (canceled)

2. (withdrawn) The circuit board of claim 1, wherein the resistive element is a resistive layer formed of a resistive material, the resistive layer between the dielectric layer and the first reference plane layer.

3. (withdrawn) The circuit board of claim 2, further comprising a second resistive layer between the dielectric layer and the second reference plane layer.

4. (withdrawn) The circuit board of claim 2, wherein the resistive layer extends substantially across and is in contact with a surface of the first reference plane layer.

5. (withdrawn) The circuit board of claim 2, further comprising a decoupling capacitor having first and second electrodes, the first electrode electrically contacted to the resistive layer and the second electrode electrically contacted to the second reference plane layer.

6. (withdrawn) The circuit board of claim 5, wherein the decoupling capacitor is between the first and second reference plane layers.

7. (withdrawn) The circuit board of claim 5, wherein the decoupling capacitor comprises a surface mount technology (SMT) capacitor embedded between the first and second reference plane layers.

8. (withdrawn) The circuit board of claim 5, wherein the decoupling capacitor has a first dimension and a second dimension less than the first dimension, the decoupling capacitor positioned such that its second dimension determines spacing between the first and second reference plane layers.

9. (withdrawn) The circuit board of claim 8, wherein the decoupling capacitor is placed on its side.

10. (withdrawn) The circuit board of claim 5, wherein the decoupling capacitor has a vertical dimension and a horizontal dimension, the decoupling capacitor positioned such that its vertical dimension determines spacing between the first and second reference plane layers.

11. (withdrawn) The circuit board of claim 5, wherein the decoupling capacitor has a first side and a second side, the first and second sides being generally parallel to each other, the first and second electrodes arranged at the first and second sides, and the decoupling capacitor positioned such that the first and second sides are generally perpendicular to main surfaces of the reference plane layers.

12. (withdrawn) The circuit board of claim 11, further comprising:

a first insulator between a first side surface of the first electrode and the resistive layer, wherein a second side surface of the first electrode is electrically connected to the second reference plane layer; and

a second insulator between a first side surface of the second electrode and the second reference plane layer, wherein a second side surface of the second electrode is electrically connected to the resistive layer.

13. (withdrawn) The circuit board of claim 2, further comprising plural decoupling capacitors between the resistive layer and the second reference plane layer.

14. (withdrawn) The circuit board of claim 13, further comprising a second resistive layer between the plural decoupling capacitors and the second reference plane layer.

15. (previously amended) A circuit board comprising:

a first reference plane layer;

a second reference plane layer;

a dielectric layer between the first and second reference plane layers;

a decoupling capacitor having first and second electrodes; and

a discrete resistor having first and second electrodes, the resistor's first electrode electrically connected to the first reference plane layer, the resistor's second electrode electrically connected to the decoupling capacitor's first electrodes, and the decoupling capacitor's second electrode electrically connected to the second reference plane layers.

16. (withdrawn) The circuit board of claim 1, further comprising a core including the first reference plane layer, second reference plane layer, dielectric layer, and resistive element.

17. (withdrawn) The circuit board of claim 16, further comprising signal layers on at least one side of the core.

18. (canceled)

19. (canceled)

20. (withdrawn) The system of claim 19, wherein a resistive element is a resistive layer formed of a resistive material, the resistive layer between the dielectric layer and the first reference plane layer.

21. (withdrawn) The system of claim 20, further comprising a second resistive layer between the dielectric layer and the second reference plane layer.

22. (withdrawn) The system of claim 20, further comprising a decoupling capacitor having first and second electrodes, the first electrode electrically connected to the resistive layer and the second electrode electrically connected to the second reference plane layer.

23. (withdrawn) The system of claim 22, wherein the decoupling capacitor is between the first and second reference plane layers.

24. (withdrawn) The system of claim 20, further comprising plural decoupling capacitors between the resistive layer and the second reference plane layer.

25. (previously amended) A system comprising:

an integrated circuit device; and

a circuit board on which the integrated circuit device is mounted, the circuit board comprising:

a first reference plane layer;

a second reference plane layer;

a dielectric layer between the first and second reference plane layers;

a decoupling capacitor having first and second electrodes; and

a discrete resistor having first and second electrodes, the discrete resistor's first electrode electrically connected to the first reference layer, the discrete resistor's second electrode electrically connected to the decoupling capacitor's first electrode, and the decoupling capacitor's second electrode electrically connected to the second reference layer.

26. (withdrawn) A method of making a circuit board, comprising:

forming first and second reference plane layers;

forming a dielectric layer between the first and second reference plane layers; and

forming a resistive element between the first and second reference plane layers.

27. (withdrawn) The method of claim 26, wherein forming the resistive element comprises forming a resistive layer between the dielectric layer and the first reference plane layer.

28. (withdrawn) The method of claim 27, further comprising forming a second resistive layer between the dielectric layer and the second reference plane layer.

29. (withdrawn) The method of claim 26, further comprising forming a core that includes the first and second reference plane layers, the dielectric layer, and the resistive element.

30. (withdrawn) The method of claim 29, further comprising forming signal layers on either side of the core.

31. (withdrawn) The method of claim 30, further comprising forming another core having first and second reference plane layers, the dielectric layer, and the resistive element.

32. (withdrawn) The method of claim 26, wherein forming the dielectric layer comprises providing a template having a plurality of holes onto the second reference plane layer.

33. (withdrawn) The method of claim 32, further comprising providing a plurality of decoupling capacitors into the holes of the template.

34. (withdrawn) The method of claim 33, further comprising attaching the first reference plane layer to another side of the template.

35. (withdrawn) The method of claim 26, further comprising providing a plurality of decoupling capacitors between the first and second reference plane layers.

36. (withdrawn) The method of claim 35, wherein providing the decoupling capacitors comprises providing surface mount technology (SMT) decoupling capacitors.

37. (withdrawn) A circuit board comprising:

a first reference plane layer;

a second reference plane layer; and

a decoupling capacitor between the first and second reference plane layers, the decoupling capacitor having a first side and a second side generally parallel to the first side, the decoupling capacitor further having a first electrode at the first side and a second electrode at the second side, the decoupling capacitor being placed on its side such that first and second sides of the decoupling capacitor are generally perpendicular to the main surfaces of the first and second reference plane layers.

(9) EVIDENCE APPENDIX

None

(10) RELATED PROCEEDINGS APPENDIX

None